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Applicant	William O'Leary
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Title: PHASE COMPARATOR FOR A PHASE LOCKED LOOP

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Appellants:	William O'Leary
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APPEAL BRIEF

Title: PHASE COMPARATOR FOR A PHASE LOCKED LOOP

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1. Introduction

On May 18, 2004 Appellants filed a notice of appeal from the final rejection of claims 1-66 set forth in the Office Action mailed March 18, 2004. Three copies of this Appeal Brief are hereby filed on July 21, 2004 and are accompanied by a fee in the amount of $330.00 as required under 37 C.F.R. §1.17(c).

2. Real Party in Interest

The real party in interest in the above-captioned application is the assignee ADC Telecommunications, Inc.

3. Related Appeals and Interferences

There are no other appeals or interferences known to Appellants which will have a bearing on the Board's decision in the present appeal.

4. Status of the Claims

Claims 1-66 are pending in the application and are the subject of this appeal. In office action mailed March 18, 2004, claims 1-5, 10-14, 19-22, 26-31, 43-44 and 64-66 were finally rejected under 35 U.S.C. §102(b) claims 6-9, 15-18, 23-24 and 33-41 were finally rejected under 35 U.S.C. §103 (a). Claims 25, 32, 42, 45, and 46-63 are allowed.

5. Status of Amendments

No amendment has been filed subsequent to the Final Office Action mailed March 18, 2004.

6. Summary of the Invention

The present invention is directed to improved phase locked loops that attenuate or eliminate spurious modulation associated with low-frequency reference clocks.

One embodiment of the invention pertains to a phase comparator (210). The phase comparator (210) comprises a phase detector (212). The phase detector (212) has a first input for receiving a first signal, a second input for receiving a second signal, and an output for providing an error signal indicative of a phase relationship between the first signal and second signal. The phase comparator (210) further comprises a digital counter (214). The digital counter (214) has a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value. The phase comparator (210) further comprises a digital-to-analog converter (216). The digital-to-analog converter (216) has an input for receiving the count value and an output for providing an error voltage signal. This embodiment is supported, for example, in figure 2, and in pages 6 - 7 of the specification.

For another embodiment, the invention provides a phase locked loop (200). The phase locked loop (200) comprises a phase comparator (210). The phase comparator (210) comprises a phase detector (212), a digital counter (214), and a digital-to-analog converter (216). The phase detector (212) has a first input for receiving a first signal, a second input for receiving a second signal, and an output for providing an error signal indicative of a phase relationship between the first signal and second signal. The digital counter (214) has a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value. The digital-to-analog converter (216) has an input for receiving the count value and an output for providing an error voltage signal. The phase locked loop (200) further comprises a filter (220). The filter (220) has an input for receiving the error voltage signal and an output for providing a control voltage signal. The phase locked loop (200) further comprises a voltage controlled oscillator (230). The voltage controlled oscillator (230) has an input for receiving the control voltage signal and an output for providing an output signal. The feedback signal is derived from the output signal. This embodiment is supported, for example, in figure 2, and in

pages 6 - 8 of the specification.

For another embodiment, the invention provides a shelf controller for controlling synchronization of shelf elements in a communications network element (500). The shelf controller includes a processor (536) and a timing circuit (300) coupled to the processor (536). The timing circuit (300) includes a first phase locked loop (306) including a phase comparator (210), a filter (220) and a voltage-controlled oscillator (230). The phase comparator (210) includes a phase detector (212) having a first input for receiving a first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal. The phase comparator (210) further includes a digital counter (214) having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value. The phase comparator (210) still further includes a digital-to-analog converter (216) having an input for receiving the count value and an output for providing an error voltage signal. The filter (220) has an input for receiving the error voltage signal and an output for providing a control voltage signal. The voltage-controlled oscillator (230) has an input for receiving the control voltage signal and an output for providing an output signal. The feedback signal is derived from the output signal. The timing circuit (300) may further include a second phase locked loop (308) having an input for receiving the second reference clock signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements, wherein the synchronization timing signal is derived from the second reference clock signal. This embodiment is supported, for example, in figures 2, 3, and 5, and in pages 6, 7, and 12 of the specification.

For yet another embodiment, the invention provides a method of generating a timing signal. The method includes generating an error signal indicative of the phase relationship between a reference clock signal and a feedback signal (405); generating a count value indicative of the amount of phase error during a single event (415); generating an error voltage signal proportional to the count value (425); and filtering the error voltage signal to produce a control voltage signal (435). The method further includes generating the timing signal in response to the

control voltage signal (445), and deriving the feedback signal from the timing signal (455). This embodiment is supported, for example, in figure 4, and in pages 12 - 14 of the specification.

For yet another embodiment, the invention provides another method of generating a timing signal. The method includes generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal (405). The error signal has a first logic state indicative of phase error between the reference clock signal and the feedback signal and a second logic state indicative of the reference clock signal and the feedback signal sharing the same phase state (p. 6 lines 24-29). The method further includes generating a count value indicative of an amount of phase error during a single period of the error signal (415). The method further includes generating an error voltage signal to produce a control voltage signal (425). The method further includes filtering the error voltage signal to produce a control voltage signal (435). The method further includes generating the timing signal in response to the control voltage signal (445). The method further includes deriving the feedback signal from the timing signal (455). This embodiment is supported, for example, in figure 4, and in pages 12 - 14 of the specification.

For still another embodiment, the invention provides a network element (500) for a communications network. The network element (500) includes a shelf backplane and a plurality of shelf elements coupled to the shelf backplane. The plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements. The at least one shelf controller includes a processor (536) and a timing circuit (300) coupled to the processor (536). The timing circuit (300) includes a phase locked loop (200). The phase locked loop (200) includes a phase comparator (210). The phase comparator (210) comprises a phase detector (212). The phase detector (212) has a first input for receiving a first signal, a second input for receiving a second signal, and an output for providing an error signal indicative of a phase relationship between the first signal and second signal. The phase detector (212) further comprises a digital counter (214). The digital counter (214) has a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value. The phase detector (212) further comprises a digital-to-analog converter (216). The

digital-to-analog converter (216) has an input for receiving the count value and an output for providing an error voltage signal. The phase locked loop (200) further includes a filter (220). The filter (220) has an input for receiving the error voltage signal and an output for providing a control voltage signal. The phase locked loop (200) further includes a voltage controlled oscillator (230). The voltage controlled oscillator (230) has an input for receiving the control voltage signal and an output. The timing circuit (300) of the shelf controller provides a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements. The synchronization timing signal is derived from the output of the voltage controlled oscillator (230). This embodiment is supported, for example, in figures 2, 3, and 5, and in pages 14 - 15 of the specification.

For another embodiment, the invention provides a phase locked loop (200). The phase locked loop (200) includes a first frequency divider. The first frequency divider has an input for receiving a first reference clock signal and an output for providing a second reference clock signal. The phase locked loop (200) further includes a phase comparator (210). The phase comparator (210) comprises a two-state phase detector (212) having a first input for receiving the second reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal indicative of a phase relationship between the second reference clock signal and the feedback signal. The phase comparator (210) further comprises a digital counter (214) having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value, wherein the count value is indicative of an amount of phase error during a single period of the error signal. The phase comparator (210) further comprises a digital-to-analog converter (216) having an input for receiving the count value and an output for providing an error voltage signal proportional to the count value. The phase locked loop (200) further includes an active filter (220) having an input for receiving the error voltage signal and an output for providing a control voltage signal, wherein the control voltage signal is representative of an average value of the error voltage signal during a period of time. The phase locked loop (200) further includes a voltage-controlled oscillator (230) having an input for receiving the control voltage signal and an output for providing an output signal.

The output signal is an oscillating signal proportional to the control voltage signal. The phase locked loop (200) further includes a second frequency divider having an input for receiving the output signal and an output for providing the feedback signal. The feedback signal has a frequency approaching a frequency of the second reference clock signal. This embodiment is supported, for example, in figure 2, and in pages 6, 7, 10, and 11 of the specification.

For another embodiment, the invention provides a method of generating a timing signal. The method includes frequency dividing a first reference clock signal by a factor of two, thereby producing a second reference clock signal having a duty cycle of approximately 50% and a frequency of approximately one-half a frequency of the first reference clock signal, generating an error signal indicative of a phase relationship between the second reference clock signal and a feedback signal using a two-state phase detector (212), generating a count value indicative of an amount of phase error during a single period of the error signal by incrementing a digital counter (214) in response to a sampling clock signal during a time when the error signal has a first logic state, passing the count value to a digital-to-analog converter (216) at a time when the error signal transitions from the first logic state to a second logic state, resetting the digital counter (214) to a selected initial value subsequent to passing the count value, generating an error voltage signal proportional to the count value using the digital-to-analog converter (216), filtering the error voltage signal using an active filter (220) to produce a control voltage signal representative of an amplified average error voltage signal, supplying the control voltage signal to a voltage-controlled oscillator (230) to generate the timing signal, and frequency dividing the timing signal to derive the feedback signal. This embodiment is supported, for example, in figure 2, and in pages 6, 7, and 10 of the specification.

For another embodiment, the invention provides a shelf controller for controlling synchronization of shelf elements in a communications network element (500). The shelf controller comprises a processor (536) and a timing circuit (300) coupled to the processor (536). The timing circuit (300) includes a first phase locked loop (306). The first phase locked loop (306) includes a phase comparator (210). The phase comparator (210) comprises a phase

detector (212) having a first input for receiving a first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal. The phase comparator (210) further comprises a digital counter (214) having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor (536), and an output for providing a count value. The phase comparator (210) further comprises a digital-to-analog converter (216) having an input for receiving the count value and an output for providing an error voltage signal. The first phase locked loop (306) further includes a filter (220) having an input for receiving the error voltage signal and an output for providing a control voltage signal and a voltage-controlled oscillator (230) having an input for receiving the control voltage signal and an output for providing a second reference clock signal. The feedback signal is derived from the second reference clock signal. The timing circuit (300) further includes a second phase locked loop (308) having an input for receiving the second reference clock signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements, wherein the synchronization timing signal is derived from the second reference clock signal. This embodiment is supported, for example, in figures 2 and 3, and in pages 12 - 15 of the specification.

For another embodiment, the invention provides a method of generating a timing signal. The method comprises generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal using a three-state phase detector (212). The error signal includes an up output and a down output (p. 10 lines 29-30). The method further comprises generating a count value indicative of an amount of phase error during a single event (415). The single event is a period between a rising edge of the reference clock signal and a next rising edge of the feedback signal when the up output is indicative of phase lead between the reference clock signal and the feedback signal. The single event is a period between a rising edge of the feedback signal and a next rising edge of the reference clock signal when the down output is indicative of phase lag between the reference clock signal and the feedback signal. The method further comprises generating an error voltage signal proportional to the count value

(425), filtering the error voltage signal to produce a control voltage signal (435), generating the timing signal in response to the control voltage signal (445), and deriving the feedback signal from the timing signal (455). This embodiment is supported, for example, in figure 4, and in pages 12 - 14 of the specification.

For another embodiment, the invention provides a network element (500) for a communications network. The network element (500) includes a shelf backplane and a plurality of shelf elements coupled to the shelf backplane. The plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements. The at least one shelf controller comprises a processor (536) and a timing circuit (300) coupled to the processor (536). The timing circuit (300) comprises a framer having an input for receiving recovered clock and data signals of a communication signal and an output for providing a first reference clock signal and a first phase locked loop (306). The first phase locked loop (306) includes a phase comparator (210). The phase comparator (210) comprises a phase detector (212) having a first input for receiving the first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal; a digital counter (214) having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor (536), and an output for providing a count value; and a digital-to-analog converter (216) having an input for receiving the count value and an output for providing an error voltage signal. The first phase locked loop (306) further includes a filter (220) having an input for receiving the error voltage signal and an output for providing a control voltage signal; and a voltage-controlled oscillator (230) having an input for receiving the control voltage signal and an output for providing a second reference clock signal. The feedback signal is derived from the second reference clock signal. The timing circuit (300) further includes a second phase locked loop (308) having an input for receiving the second reference clock signal and an output for providing a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements, wherein the synchronization timing signal is derived from the second reference clock signal. The timing circuit (300) further comprises a

second phase locked loop (308). The second phase locked loop (308) has an input for receiving the second reference clock signal and an output for providing a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements. The synchronization timing signal is derived from the second reference clock signal. This embodiment is supported, for example, in figure 5, and in pages 6, 7, 14, and 15 of the specification.

For another embodiment, the invention provides a shelf controller for controlling synchronization of shelf elements in a communications network element (500). The shelf controller comprises a processor (536) and a timing circuit (300) coupled to the processor (536). The timing circuit (300) includes a phase locked loop (200). The phase locked loop (200) comprises a phase comparator (210). The phase comparator (210) includes a phase detector (212) having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal; a digital counter (214) having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor (536), and an output for providing a count value; and a digital-to-analog converter (216) having an input for receiving the count value and an output for providing an error voltage signal. The phase comparator (210) further includes a voltage-controlled oscillator (230) having an input coupled to receive the error voltage signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements. The feedback signal is derived from the output of the voltage-controlled oscillator (230). This embodiment is supported, for example, in figures 2, 3, and 5, and in pages 6, 7, 12, 14, and 15 of the specification.

Another embodiment of the invention provides a network element (500) for a communications network. The network element (500) comprises a shelf backplane and a plurality of shelf elements coupled to the shelf backplane. The plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements. The at least one shelf controller comprises a processor (536) and a timing circuit (300) coupled to the processor (536). The timing circuit (300) comprises a phase locked loop (200).

The phase locked loop (200) comprises a phase comparator (210). The phase comparator (210) includes a phase detector (212) having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal; a digital counter (214) having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor (536), and an output for providing a count value; and a digital-to-analog converter (216) having an input for receiving the count value and an output for providing an error voltage signal. The phase locked loop (200) further comprises a voltage-controlled oscillator (230) having an input coupled to receive the error voltage signal and an output. The timing circuit (300) provides a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements. The synchronization timing signal is derived from the output of the voltage-controlled oscillator (230). This embodiment is supported, for example, in figures 2 and 5, and in pages 6, 7, 12, 14, and 15 of the specification.

Another embodiment of the invention provides a method of generating a timing signal. The method comprises generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal (405); adjusting a value of a counter a plurality of times during a single event to produce a value indicative of an amount of phase error during the single event (p. 8 lines 5-9); generating an error voltage signal proportional to the count value (425); generating the timing signal in response to the error voltage signal (435); and deriving the feedback signal from the timing signal (455). This embodiment is supported, for example, in figure 4, and in pages 12-14 of the specification.

Another embodiment of the invention provides a method of generating a timing signal. The method comprises generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal (405); generating a sampling clock signal to define a plurality of sampling intervals (p. 8 lines 5-7); adjusting a value of a counter during sampling intervals for a single event based on the sampling clock to produce a value indicative of an amount of phase error during the single event (p. 8 lines 5-7); generating an error voltage signal proportional to the count value (425); generating the timing signal in response to the error

voltage signal (445); and deriving the feedback signal from the timing signal (455). This embodiment is supported, for example, in figure 4, and in pages 12-14 of the specification.

7. Issues Presented for Review

The first question presented in this Appeal is whether the Examiner erred in rejecting claims 1-5, 10-14, 19-22, 26-31, 43-44, and 64-66 under 35 USC § 102(b) as being anticipated by McCauley (U.S. Patent No. 4,847,678).

The second question presented in this Appeal is whether the Examiner erred in rejecting claims 6-9, 15-18, 23-24, and 33-41 under 35 USC § 103(a) as being anticipated by McCauley (U.S. Patent No. 4,847,678) in view of Tekeuchi (U.S. Patent No. 5,727,193).

The third question presented in this Appeal is whether the examiner erred in objecting to the drawings as failing to show all of the claimed features.

8. Grouping of Claims

Each of claims 1-66 stands or falls on their own merits for reasons detailed below. Each of the claims is patentably distinct for the reasons detailed below.

9. Arguments

A. Rejections of claims 1-5, 10-14, 19-22, 26-31, 43-44 and 64-66 under 35 U.S.C. §102 (b)

1. The Applicable Law

35 U.S.C. §102 provides in relevant part:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A claim is anticipated under 35 U.S.C.§ 102 only if each and every element as set forth in

the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but identical terminology is not required. *In re Bond,* 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberyl-Clark Corp.,* 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.,* 75 F.3d 1558, 37 U.S.P.Q.2d 1618 (Fed. Cir. 1996).

2. 35 U.S.C. § 102(b) rejection analysis

Claims 1-5, 10-14, 19-22, 26-31, 43-44 and 64-66 were rejected under 35 U.S.C. §102 (b) as being anticipated by McCauley (U.S. Patent No. 4,847,678). Claim 1 of the present application is directed to a "phase comparator" that recites, in relevant part, "a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value . . . ."

The Examiner erred in rejecting claim 1 under 35 USC § 102(b). In particular, McCauley does not teach a "phase comparator, comprising: . . . a digital counter having . . . a second input for receiving a sampling clock signal," as recited in claim 1.

The Examiner took the position that the phase error (item 51 in Fig. 2) received by the up/down counter (item 52 in Fig. 2) of McCauley is equivalent to the sampling clock signal received by the digital counter in the present invention. The Examiner, in the Final Office Action, cited column 5, lines 12-25 and lines 56-61 as well as column 7, lines 47-62 in rejecting claim 1 of the present application. Column 5, lines 12-25 reads:

> [U]pon initial power up of the system, a quantity midway between zero and the counter's maximum count is loaded into the counter. If the phase detector determines that the burst information leads the PLL reference signal VREF, for example, then the counter is placed in the up counting mode by the PHASE SIGN output, and is clocked up by the PHASE ERROR output. This speeds up the oscillator. On the other hand, if the phase detector determines that horizontal sync information, for example, lags VREF, then the counter is placed in a down counting mode by PHASE SIGN and it is clocked down by the PHASE ERROR output. This slows down the oscillator.

Column 5, lines 56-61 reads:

> Continuing downstream in Fig. 2, conversion of the digital output from counter to an analog signal is accomplished by a D/A converter whose output is fed to the input of VCO causing it to speed up or slow down depending on whether the counter is counting up or down.

Column 7, lines 47-62 reads:

> Continuing with the discussion of the PLL, the counter is described in greater detail in Fig. 7. In an exemplary embodiment, the counter includes a pair of cascaded counters 120a, 120b, such as two 74AS169 counters. The LOADCOUNT (pins 9) of the counters are tied to a conventional power up reset circuit which loads a count having a value which is one half of the maximum count. Up or down counting is controlled by the PHASE SIGN input to pins 1, while the clocks are tied to the PLL phase detector PHASE ERROR output. The counter 120a, which generates the least significant nibble of the count, is enabled by the B or H window output form detector to pin 7, while the counter 120b, which generates the most significant nibble, is enabled (sic) by the ripple carry output (RCO) from counter 120a.

None of the cited paragraphs succeed in establishing an equivalency between the PHASE ERROR output of McCauley and the sampling clock signal of the present invention. More particularly, the term "sampling clock signal" has special meaning in the art. The term "sampling" is defined as "[a] technique in which only some portions of an electrical signal are measured and are used to produce a set of discrete values that is representative of the information contained in the whole." *The New Penguin Dictionary of Electronics,* 500 (2d ed. 1988). A

sampling clock is used to derive the set of instantaneous values during a sampling process. Thus, in claim 1, the term "sampling clock signal" carries with it the meaning that it is a clock signal that is used to gather a plurality of values during a given sampling period. There is nothing in McCauley that teaches or suggests this limitation of claim 1. For example, McCauley shows in Figures 4A and 4B that the phase error signal (provided to the clock input of counter 52) provides exactly one pulse during the measurement window. Col. 4, lines 29-51 and Col. 5, lines 26-55. McCauley further states, with reference to Fig. 4a:

> [T]he oscillator output VREF leads the color burst, i.e. the leading edge of VREF leads the leading edge of the windowed burst, then the EXOR gate output (PHASE SIGN) is a logic low (as indicated by the arrow) during the presence of the windowed PHASE ERROR pulse, which causes the counter to count down one increment, and in turn to generate a lower frequency output from VCO.

Col. 6, lines 23-31. During a windowed burst, the up/down counter is only capable of counting up or down by one increment, in accordance to the phase error and phase sign inputs. In the quoted example above, a down increment is generated in the up/down counter. However, all embodiments of McCauley, whether counting up or down, are capable of only one incremental count per event. See col. 6, lines 62-64, lines 36-41, and col. 7, lines 21-24. This is not a sampling clock as called for in claim 1.

The examiner states that the definition of sampling provided by the applicant does not apply to the digital counter of Figure 2. P. 7, paragraph 8 of Office Action. Applicant respectfully traverses this rejection. Applicant's use of the term "sampling" is described in the specification of the present application. In Figure 2, the digital counter acts as a "sampling" device because it samples the amount of phase error between the reference clock signal and the feedback signal. The greater the error, the higher the digital counter counts. The examiner's indication that a digital counter cannot be used as a sampling device actually supports Applicant's claim of a patentable invention. Examiner's comment appears to reflect the feeling in the art that a digital counter cannot be used as a sampling device. If true, Applicant's claimed use of a digital counter in this manner cannot be said to be obvious, let alone anticipated!

The examiner further asserts that McCauley shows a digital counter having a second input for receiving a sampling clock signal. As explained above though, the second input of counter 52 in McCauley has a second input for receiving a phase error signal, which is distinct from a sampling clock signal. The phase error signal can not be interpreted as a sampling clock signal as herein defined, given that the phase error signal transmits only one pulse per measurement period or window. See col. 6, lines 62-64, lines 36-41, and col. 7, lines 21-24.

The examiner states that it is irrelevant whether McCauley discloses providing exactly one pulse during a measurement window. However, the fact that only one pulse is provided shows that the phase error signal cannot be a sampling clock signal as herein defined. Therefore this fact is relevant, and further indicates the inventive nature of the claimed invention.

Examiner further states that according to applicant's understanding of McCauley's PLL, McCauley's PLL would not be able to properly lock onto a signal. However, applicant merely asserts that McCauley's PLL locks onto a signal in a different manner than the present invention. In McCauley, a feedback signal is compared to a reference signal to generate a phase sign signal and a phase error signal. Col. 5, lines 1-12. The phase sign and phase error signal are input into an up/down counter that is incremented once. Col. 5, lines 13-26. The value of the up/down counter is then sent to the D/A converter, converted to an analog signal, and the VCO is changed by a slight amount. This is repeated until the VCO's phase matches the phase of the reference signal.

In contrast, the invention as called for in claim 1 outputs an error signal indicative of a phase relationship between the first signal and second signal. This error signal is input into a digital counter along with a sampling clock signal to generate a count value. The count value is indicative of the phase difference between the first signal and second signal.

The claimed invention offers the advantage that the phase difference between the feedback signal and reference clock signal can be aligned in a reduced amount of time. This is more critical in applications such as communications systems, wherein delays can result in noticeable degradation of a transmitted signal. In contrast, McCauley is designed for applications such as synchronizing video signals that have less restrictive requirements, for

example due to the refresh rate of the human eye. Col. 3, lines 51-53. In McCauley, synchronization occurs on either the horizontal sync pulse, or on the color burst. Col. 3, lines 56-68 and col. 4, lines 1-4. However, the horizontal sync pulse and color burst are not synchronized. In fact, "the leading edge of the color burst . . . corresponds to the leading edge of the horizontal sync pulse within a tolerance of plus or minus forty degrees, which is within RS-170A specifications adopted by the U.S. Government for transmission of color video." Col. 5, lines 41-46. Therefore a synchronization difference of plus or minus forty degrees is tolerated in McCauley. Such a variation in synchronization does not occur in the invention as claimed in claim 1. Additionally, though it can be used for high frequency applications, the invention of claim 1 was provided to address problems associated with synchronization of low frequency signals. Application, P. 5, lines 29-30, P. 6, lines 1-6. In contrast, the invention of McCauley was provided to address synchronization of high frequency imaging devices. Col. 3, lines 51-55. Therefore, claim 1 is not anticipated by McCauley.

Claims 2-5 depend from and include the patentable limitations of claim 1 and are thus also allowable. Additionally, claim 2 discloses further limitations that make it allowable under its own merits. Claim 2 discloses, "wherein the error signal has a first logic state indicative of a phase error between the first signal and second signal." While the error signal has the first logic state, the sampling clock signal is received at the digital counter. Therefore, for example, the first logic state can be viewed as a window during which sampling occurs.

Claim 10 also include the limitation that the digital counter receives a sampling clock input signal. Therefore, for the reasons identified above with respect to claim 1, claim 10 is also not anticipated by McCauley.

Claims 11-14 and 19-22 depend from claim 10 and are thus also allowable.

Claim 26 reads as follows:

> 26. A method of generating a timing signal, comprising:
>
> generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal;

> generating a count value indicative of an amount of phase error during a single event;
>
> generating an error voltage signal proportional to the count value;
>
> filtering the error voltage signal to produce a control voltage signal;
>
> generating the timing signal in response to the control voltage signal; and
>
> deriving the feedback signal from the timing signal.

In part, claim 26 requires that the error signal generated is "proportional to the count value" and that the count value is "indicative of an amount of phase error during a single event." This is not true with the count in McCauley. In McCauley, each event results in incrementing or decrementing the counter once. Col. 6, lines 10-41. Since the amount by which the counter is incremented is not related to the amount of phase difference, the count value is not "indicative of an amount of phase error during a single event." Therefore, claim 26 is not anticipated by McCauley.

Claims 27, 29, and 30 depend from claim 26 and are thus also allowable.

Claim 28 depends from claim 27 and is thus also allowable. Further, claim 28 also specifies:

> wherein generating a count value comprises incrementing a digital counter in response to a sampling clock signal during a time when the error signal has a first logic state and wherein generating an error voltage occurs at a time when the error signal transitions from the first logic state to a second logic state

This limitation is missing from McCauley because McCauley does not show a sampling clock and does not show incrementing a counter in response to a sampling clock during the time an error signal has a first logic state. Therefore, claim 28 is not anticipated by McCauley.

Claims 31 and 43 include similar limitations as discussed above with respect to claim 26 and are thus also allowable for the same reasons.

Claim 44 depends from claim 43 and is thus similarly allowable. Further, claim 44 adds a limitation with respect to incrementing and decrementing a counter in response to a sampling clock signal. As discussed above, McCauley does not teach or suggest a sampling clock signal. Therefore, claim 44 is not anticipated by McCauley.

B. Rejection of claims 6-9, 15-18, 23-24 and 33-41 under 35 U.S.C. §103(a)

1. Applicable Law

35 U.S.C.§ 103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

To establish a case of *prima facie* obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based in the applicant's disclosure. *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir 1991). MPEP § 2143 - § 2143.03.

2. 35 U.S.C. § 103(a) Rejection Analysis

Claims 6-9, 15-18, 23-24 and 33-41 were rejected under 35 U.S.C.§ 103 (a) as being unpatentable over McCauley (U.S. Patent No. 4,847,678) in view of Takeuchi (U.S. Patent No. 5,727,193).

Claims 6-8 depend from claim 1 and add limitations directed to aspects of the sampling

clock signal. The Examiner rejected these claims stating that the limitations of these claims "recite obvious variations of well known timing and synchronization procedures and circuitry and would have been obvious in view of the teachings and suggestions" of the references. The Examiner points to no specific teachings to support this statement. Therefore, Applicant respectfully traverses the statement and requests that the Examiner withdraw the statement or provide a reference and citation to back-up this assertion in the next action. Applicant respectfully asserts that there is nothing in either reference that teaches or suggests these limitations on the sampling clock signal. As discussed above with respect to claim 1, the primary reference fails to teach or suggest a sampling clock signal. Those arguments are incorporated herein by reference. Applicant respectfully asserts that there is nothing in the secondary reference, alone or in combination with the primary reference, that teaches or suggests the use of a sampling clock signal or the additional limitations found in claims 6-8. Therefore, claims 6-8 are not obvious in light of the art.

Claim 9 also depends from claim 1. Claim 9 adds limitations on the resolution of the counter and the digital-to-analog converter. The Examiner rejected claim 9 with the same statement used in rejecting claims 6-8. Again, Applicant respectfully asserts that this rejection is not proper as the Examiner has provided no basis for the assertion. Applicant respectfully requests that the rejection be dropped or a reference be provided that demonstrate that these limitations are obvious variations. There is no discussion in either of the references, taken alone or in combination, that addresses the issue of the resolution of these elements. Therefore, claim 9 is also not obvious in light of the references.

Claims 15-17 depend from claim 10 and add similar limitations as claims 6-8 added to claim 1. Therefore, claims 15-17 are also allowable for the reasons identified above with respect to claims 6-8.

Claim 18 depends from claim 10 and adds a similar limitation as claim 9 added to claim 1. Therefore, claim 18 is also allowable for the reasons provided above with respect to claim 9.

Claims 23 and 24 depend from independent claim 10 discussed above. There is nothing in the combination of McCauley and Takeuchi that teaches or suggests the limitation missing

from claim 10 as discussed above. Therefore, claims 23 and 24 are also not taught or suggested by the references, alone or in combination.

Claims 33 and 40 were rejected for the reasons identified with respect to claims 10, 11, 19, 22, and 23. Applicant respectfully asserts that claims 33 and 40 are allowable based on the arguments above with respect to claims 10, 11, 19, 22, and 23.

Claims 34-39 and 41 were rejected based on the reasons applied to claims 12, 13, 15, 20, 22, and 24. Applicant respectfully asserts that claims 34-39 and 41 are allowable based on the arguments above with respect to claims 12, 13, 15, 20, 22, and 24.

C. Rejection of drawings under 35 U.S.C. §113

1. Applicable Law

35 U.S.C.§ 113 provides in relevant part:

> The applicant shall furnish a drawing where necessary for the understanding of the subject matter to be patented. When the nature of such subject matter admits of illustration by a drawing and the applicant has not furnished such a drawing, the Commissioner may require its submission within a time period of not less than two months from the sending of a notice thereof.

2. 35 U.S.C. § 113 Rejection Analysis

The examiner erred in objecting to the drawings. Particularly, the examiner objected to the drawings for failure to show all of the claimed features, including a phase detector that is a two-state phase detector that uses XOR logic, a phase detector that is a two state phase detector that is a sequential phase detector, and a phase detector that is a three-state phase detector, as recited in the claims. These elements are shown in element 212 of Figure 2 as described in the specifications at p. 6, lines 25-29 and p. 11, lines 3-4.

Examiner has refuted that element 212 of Figure 2 does not show the above stated limitations, as recited in the claims, stating that element 212 is merely a box labeled "Phase Detector." The applicant respectfully traverses these objections. A person of ordinary skill in

the art would be able to build the invention as shown in Figure 2 based on Figure 2 and the accompanying explanation in the specification. A person of ordinary skill in the art understands what a phase detector comprises and how it is designed for a two-state phase detector that uses XOR logic, a two state sequential phase detector, and a three state phase detector. Therefore, element 212 of Figure 2 shows the limitations of the claims with enough detail to enable one of ordinary skill in the art to construct the disclosed invention. Withdrawal of the objection is respectfully requested.

10. Summary

Appellants have set forth reasons why the Examiner is incorrect in maintaining the rejections of the pending claims. Specifically, the Examiner has failed to set forth a prima facie case of anticipation or obviousness. McCauley and Takeuchi either alone or in combination do not teach all of the limitations in the pending independent and dependant claims. Appellant respectfully submits that, for the above reasons, Claims 1-66 are allowable over the cited art. Therefore, reversal of the Examiner's rejections is respectfully requested.

Respectfully submitted,

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Appendix 1

The Claims on Appeal

1. A phase comparator, comprising:

a phase detector having a first input for receiving a first signal, a second input for receiving a second signal, and an output for providing an error signal indicative of a phase relationship between the first signal and the second signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal.

2. The phase comparator of claim 1, wherein the phase detector is a two-state phase detector and wherein the error signal has a first logic state indicative of a phase error between the first signal and the second signal.

3. The phase comparator of claim 2, wherein the two-state phase detector is an XOR logic gate.

4. The phase comparator of claim 2, wherein the two-state phase detector is a two-state sequential phase detector.

5. The phase comparator of claim 1, wherein the phase detector is a three-state phase detector and wherein the error signal has a first output indicative of phase lead between the

first signal and the second signal, and a second output indicative of phase lag between the first signal and the second signal.

6. The phase comparator of claim 1, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

7. The phase comparator of claim 1, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

8. The phase comparator of claim 1, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

9. The phase comparator of claim 1, wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

10. A phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing an output signal, wherein the feedback signal is derived from the output signal.

11. The phase locked loop of claim 10, wherein the phase detector is a two-state phase detector.

12. The phase locked loop of claim 11, wherein the two-state phase detector is an XOR logic gate.

13. The phase locked loop of claim 11, wherein the two-state phase detector is a two-state sequential phase detector.

14. The phase locked loop of claim 10, wherein the phase detector is a three-state phase/frequency phase detector.

15. The phase locked loop of claim 10, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

16. The phase locked loop of claim 10, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

17. The phase locked loop of claim 10, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

18. The phase locked loop of claim 10 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

19. The phase locked loop of claim 10 wherein the filter further comprises an active filter.

20. The phase locked loop of claim 10 wherein the voltage-controlled oscillator is a voltage-controlled crystal oscillator.

21. The phase locked loop of claim 10 wherein the feedback signal is the output signal of the voltage-controlled oscillator.

22. The phase locked loop of claim 10 further comprising a frequency divider coupled between the output of the voltage-controlled oscillator and the second input of the phase detector, wherein the frequency divider comprises a divide-by-N block and wherein a target frequency of the output signal of the voltage-controlled oscillator is approximately N times a frequency of the first reference clock signal.

23. The phase locked loop of claim 10 further comprising:

a frequency divider having an input for receiving a second reference clock signal and an output for providing the first reference clock signal as a selected fraction of the second reference clock signal.

24. The phase locked loop of claim 23, wherein the frequency divider comprises a divide-by-two block, thereby producing a first reference clock signal having a 50% duty cycle and a frequency of approximately one-half of a frequency of the second reference clock signal.

25. A shelf controller for controlling synchronization of shelf elements in a communications network element, the shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements, wherein the feedback signal is derived from the output of the voltage-controlled oscillator.

26. A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal;

generating a count value indicative of an amount of phase error during a single event;

generating an error voltage signal proportional to the count value;

filtering the error voltage signal to produce a control voltage signal;

generating the timing signal in response to the control voltage signal; and

deriving the feedback signal from the timing signal.

27. The method of claim 26, wherein generating an error signal comprises generating an error signal with a two-state phase detector and wherein the single event comprises a single period of the error signal.

28. The method of claim 27, wherein generating a count value comprises incrementing a digital counter in response to a sampling clock signal during a time when the error signal has a first logic state and wherein generating an error voltage occurs at a time when the error signal transitions from the first logic state to a second logic state.

29. The method of claim 26, wherein generating the timing signal comprises applying the control voltage to a voltage-controlled oscillator.

30. The method of claim 26, wherein deriving the feedback signal from the timing signal comprises dividing the feedback signal by a selected factor N, wherein the timing signal has a target frequency of approximately N times a frequency of the reference clock signal.

31. A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal, wherein the error signal has a first logic state indicative of phase error between the reference clock signal and the feedback signal and a second logic state indicative of the reference clock signal and the feedback signal sharing the same phase state;

generating a count value indicative of an amount of phase error during a single period of the error signal;

generating an error voltage signal proportional to the count value;

filtering the error voltage signal to produce a control voltage signal;

generating the timing signal in response to the control voltage signal; and

deriving the feedback signal from the timing signal.

32. A network element for a communications network, the network element comprising:

a shelf backplane; and

a plurality of shelf elements coupled to the shelf backplane, wherein the plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements, the at least one shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output;

wherein the timing circuit provides a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements; and

wherein the synchronization timing signal is derived from the output of the voltage-controlled oscillator.

33. A phase locked loop, comprising:

a first frequency divider having an input for receiving a first reference clock signal and an output for providing a second reference clock signal;

a phase comparator, comprising:

a two-state phase detector having a first input for receiving the second reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal indicative of a phase relationship between the second reference clock signal and the feedback signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value, wherein the count value is indicative of an amount of phase error during a single period of the error signal; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal proportional to the count value;

an active filter having an input for receiving the error voltage signal and an output for providing a control voltage signal, wherein the control voltage signal is representative of an average value of the error voltage signal during a period of time;

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing an output signal, wherein the output signal is an oscillating signal proportional to the control voltage signal; and

a second frequency divider having an input for receiving the output signal and an output for providing the feedback signal, wherein the feedback signal has a frequency approaching a frequency of the second reference clock signal.

34. The phase locked loop of claim 33, wherein the two-state phase detector is an XOR logic gate.

35. The phase locked loop of claim 33, wherein the two-state phase detector is a two-state sequential phase detector.

36. The phase locked loop of claim 33, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

37. The phase locked loop of claim 33, wherein the voltage-controlled oscillator is a voltage-controlled crystal oscillator.

38. The phase locked loop of claim 33, wherein the first frequency divider comprises a divide-by-two block, thereby producing the second reference clock signal having a 50% duty cycle and a frequency of approximately one-half of a frequency of the first reference clock signal.

39. The phase locked loop of claim 38, wherein the output signal of the voltage-controlled oscillator has a frequency that is a selected multiple N of the frequency of the first reference clock signal, and wherein the second frequency divider comprises a divide-by-N block followed by a divide-by-two block, thereby producing the feedback signal having a 50% duty cycle and a frequency approaching the frequency of the second reference clock signal.

40. A method of generating a timing signal, comprising:

frequency dividing a first reference clock signal by a factor of two, thereby producing a second reference clock signal having a duty cycle of approximately 50% and a frequency of approximately one-half a frequency of the first reference clock signal;

generating an error signal indicative of a phase relationship between the second reference clock signal and a feedback signal using a two-state phase detector;

generating a count value indicative of an amount of phase error during a single period of the error signal by incrementing a digital counter in response to a sampling clock signal during a time when the error signal has a first logic state;

passing the count value to a digital-to-analog converter at a time when the error signal transitions from the first logic state to a second logic state;

resetting the digital counter to a selected initial value subsequent to passing the count value;

generating an error voltage signal proportional to the count value using the digital-to-analog converter;

filtering the error voltage signal using an active filter to produce a control voltage signal representative of an amplified average error voltage signal;

supplying the control voltage signal to a voltage-controlled oscillator to generate the timing signal; and

frequency dividing the timing signal to derive the feedback signal.

41. The method of claim 40, wherein frequency dividing the timing signal comprises first dividing the timing signal by a selected factor N, wherein the timing signal has a target frequency of approximately N times a frequency of the first reference clock signal, then dividing the resulting signal by a factor of two, thereby producing a feedback signal having a duty cycle of approximately 50% and a frequency approaching the frequency of the second reference clock signal.

42. A shelf controller for controlling synchronization of shelf elements in a communications network element, the shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a first phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing a second reference clock signal, wherein the feedback signal is derived from the second reference clock signal; and

a second phase locked loop having an input for receiving the second reference clock signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements, wherein the synchronization timing signal is derived from the second reference clock signal.

43. A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal using a three-state phase detector, wherein the error signal includes an up output and a down output;

generating a count value indicative of an amount of phase error during a single event, wherein the single event is a period between a rising edge of the reference clock signal and a next rising edge of the feedback signal when the up output is indicative of phase lead between the reference clock signal and the feedback signal and wherein the single event is a period between a rising edge of the feedback signal and a next rising edge of the reference

clock signal when the down output is indicative of phase lag between the reference clock signal and the feedback signal;

generating an error voltage signal proportional to the count value;

filtering the error voltage signal to produce a control voltage signal;

generating the timing signal in response to the control voltage signal; and

deriving the feedback signal from the timing signal.

44. The method of claim 43, wherein generating a count value indicative of an amount of phase error further comprises setting a digital counter to an initial value and incrementing the digital counter in response to a sampling clock signal during the single event when the up output is indicative of phase lead between the reference clock signal and the feedback signal and setting the digital counter to the initial value and decrementing the digital counter in response to the sampling clock signal during the single event when the down output is indicative of phase lag between the reference clock signal and the feedback signal.

45. A network element for a communications network, the network element comprising:

a shelf backplane; and

a plurality of shelf elements coupled to the shelf backplane, wherein the plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements, the at least one shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a framer having an input for receiving recovered clock and data signals of a communication signal and an output for providing a first reference clock signal;

a first phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving the first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing a second reference clock signal, wherein the feedback signal is derived from the second reference clock signal; and

a second phase locked loop having an input for receiving the second reference clock signal and an output for providing a synchronization timing signal to the shelf backplane for the

synchronization of the plurality of shelf elements, wherein the synchronization timing signal is derived from the second reference clock signal.

46. The shelf controller of claim 25, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

47. The shelf controller of claim 25, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

48. The shelf controller of claim 25, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

49. The shelf controller of claim 25 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

50. The network element of claim 32, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

51. The network element of claim 32, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

52. The network element of claim 32, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

53. The network element of claim 32 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

54. The shelf controller of claim 42, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

55. The shelf controller of claim 42, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

56. The shelf controller of claim 42, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

57. The shelf controller of claim 42 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

58. The network element of claim 45, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

59. The network element of claim 45, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

60. The network element of claim 45, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

61. The network element of claim 45 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

62. A shelf controller for controlling synchronization of shelf elements in a communications network element, the shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal; and

a voltage-controlled oscillator having an input coupled to receive the error voltage signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements, wherein the feedback signal is derived from the output of the voltage-controlled oscillator.

63. A network element for a communications network, the network element comprising:

a shelf backplane; and

a plurality of shelf elements coupled to the shelf backplane, wherein the plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements, the at least one shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling

clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal; and

a voltage-controlled oscillator having an input coupled to receive the error voltage signal and an output;

wherein the timing circuit provides a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements; and

wherein the synchronization timing signal is derived from the output of the voltage-controlled oscillator.

64. A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal;

adjusting a value of a counter a plurality of times during a single event to produce a value indicative of an amount of phase error during the single event;

generating an error voltage signal proportional to the count value;

generating the timing signal in response to the error voltage signal; and

deriving the feedback signal from the timing signal.

65. The method of claim 64, wherein adjusting a value of the counter a plurality of times comprises adjusting the counter using a sampling clock signal.

66. A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal;

generating a sampling clock signal to define a plurality of sampling intervals;

adjusting a value of a counter during sampling intervals for a single event based on the sampling clock to produce a value indicative of an amount of phase error during the single event;

generating an error voltage signal proportional to the count value;

generating the timing signal in response to the error voltage signal; and

deriving the feedback signal from the timing signal.